

## REMARKS

The Examiner is thanked for conducting a personal interview with Applicant's representative on January 7, 2009, and for suggesting the above amendments, which are believed to overcome the cited prior art as discussed during the interview.

Reconsideration of the pending application is respectfully requested on the basis of the following particulars:

1. Amendments and Support for Same

By the Response, claim 1 has been amended to further clarify the features of claimed invention and more particularly point out and distinctly claim the subject matter of the invention. No new matter has been added. Accordingly, claims 1-5 are respectfully submitted for consideration. Approval and entry of the amendments are respectfully requested.

2. Rejection under 35 U.S.C. §102(b)

With respect to the rejection of claims 1-5 under 35 U.S.C. §102(b) as being anticipated by Hathaway (US 6,536,024), in spite of the above-presented amendments to overcome Hathaway, Applicant respectfully traverses the rejection for the record at least for the reason that Hathaway fails describe each and every limitation recited in the rejected claims.

The present invention directed to a method of designing semiconductor ICs comprises two separate routines, as shown in Fig. 2 of the application. According to Fig. 2, a first routine SUB1 is a circuit design routine. Following the completion of the circuit design routine is a layout design routine SUB2.

Claim 1 generally is directed to the circuit design routine SUB1, which is shown in details as substeps (e.g., SS16, SS20, SS22, and SS24) in Fig. 3, while dependent claim 2 is directed to the sequential layout design routine SUB2 shown in details as substeps (e.g.,

SS34, SS36, SS38, SS40, and SS42) in Fig. 4.

Applicant respectfully submits that the steps in SUB1 in Fig. 3 are performed before the steps in SUB2 in Fig. 4. Hence, the claimed steps 1<sup>st</sup> through 7<sup>th</sup> steps in claims 1 and 2 are performed in proper order as recited in the claims.

With Applicant's claimed method as recited in the steps of claims 1 and 2, for example, timing analysis is performed using the plural clocks even in the layout design (i.e., SUB2 steps) to make decision as to whether violation of timing constraints has occurred, thereby making it possible to obtain layout design that has satisfied all constraints, as discussed in lines 3-8 in page 20 of the specification.

The disclosure in lines 9-26 in page 20 of the specification further discusses additional advantages of the claimed invention over known art, as follows:

“According to the circuit design and the layout design, the number of the clock trees and the differences in delay among the respective clock trees are determined from the result of the timing analysis on the gate level net list of the tentative logic combination result. Further, the clock tree that satisfies the sampling timing of each flip-flop circuit is selected and used. Therefore, the logic combination, which has been executed by uniformly placing the same timing constraint on the logic paths, results in a logic combination to which constraints on the timings corresponding to the lengths of the paths are applied. Applying the individual timing constraints and combining them makes it possible to relax a corresponding path strict with respect to timing constraints from the early stage of the circuit design and to obtain a semiconductor integrated circuit that satisfies a higher operating speed as compared with the normal circuit design.”

Regarding the obviousness rejection, particularly sections 4 and 5 in pages 2 and 3 of the Office Action, the Examiner relies mainly on Fig. 2b of Hathaway as describing both the circuit design routine steps and circuit design routine steps recited in Applicant's claims 1 and 2, respectively. In response, Applicant respectfully asserts that Fig. 2b of Hathaway is generally directed to a method for optimized placement of clock sinks and logic circuitry wherein all of the sinks of each domain are placed into one or more clusters on the chip as depicted in FIG. 2a-i and FIG. 2a-ii of Hathaway. That is, Hathaway does not describe similar steps of claims 1 and 2 of the Applicant's invention, and the flow chart in Fig. 2b of Hathaway does not encompass all of the claimed steps 1<sup>st</sup> through 7<sup>th</sup> recited in claims 1 and 2 of the present invention.

Applicant respectfully asserts that Fig. 2b of Hathaway does not appear to have detailed descriptions in the specification describing the flow diagram in Fig. 2b to support the Examiner's allegation that Hathaway actually describes Applicant's 1<sup>st</sup> step through 7<sup>th</sup> step in claims 1 and 2 of the present invention. Further, taken the process shown in Fig. 2b in correct context and order as shown, Hathaway does not describe all of Applicant's claimed 1<sup>st</sup> through 7<sup>th</sup> steps in claims 1 and 2, for example.

Particularly, in equating Hathaway's element 212 (Create a Skeleton Clock Tree) as Applicant's 1<sup>st</sup> and 2<sup>nd</sup> claimed step, and Hathaway's element 216 (If a Domain has been Split into Separate Subdomains, Update the Domain's Clock Net's Netlist) as Applicant's 3<sup>rd</sup> claimed step, the Examiner has taken the elements 212 and 216 completely out of context by ignoring the other essential intermediate elements 213 (Establish a Target Condition), 214 (Determining Compliance of a Domain with a Target Condition), and 215 (Perform Placement Step) in Fig. 2b of Hathaway.

Further, the Examiner alleges that elements 214 and 217 of Hathaway are equivalent to Applicant's 4<sup>th</sup> step, and that element 217 of Hathaway is also equivalent to Applicant's 6<sup>th</sup> step. However, Applicant respectfully submits that it is simply not technically possible for both elements 214 and 217 of Hathaway to be equivalent to Applicant's 4<sup>th</sup> step, and the element 217 of Hathaway to be equivalent to Applicant 6<sup>th</sup> step without completely destroying the intended method in the flow chart in Fig. 2b of Hathaway.

Further, Applicant respectfully submits that the Examiner merely alleges that Hathaway discloses Applicant's 5<sup>th</sup> step of adjusting skews without showing where in Fig. 2b that such an equivalent feature may be found. Instead, the Examiner improperly relies on col. 31, lines 18-24 of Hathaway as disclosing adjusting skews. However, the skew adjustment described in col. 31, lines 18-24 of Hathaway does not appear to be related to any of the process step shown in Fig. 2b of Hathaway. Hence, should the Examiner continue to contend Fig. 2b as showing Applicants steps 1-4 and 6-7, as well as step 5 for adjusting skews for each the clocks, Applicant would respectfully request the Examiner to show the connection between col. 31, lines 18-24 and Figs. 2b of Hathaway and how skew adjustment fits in with the steps shown in the flow chart of Fig. 2b of Hathaway which are directed to optimizing placement of clock sinks and logic circuitry, wherein all of the sinks of each domain are placed into one or more clusters on a chip.

Applicant respectfully submits that claims 1 and 2 of the present invention recite a number of steps taken in a sequence and combination that constitutes a process, and, unlike Applicant's claimed steps, the steps in Fig 2b of Hathaway do not follow the sequential or even logical order or include the combination of steps as Applicants' claimed invention. That is, the Examiner selected various features of Hathaway that are not relevant to Applicant's claimed steps and mischaracterized as equivalent to Applicant's claimed steps.

Applicant respectfully submits that, although Examiners are entitled to interpreting a reference broadly, the reference's teaching may not be taken out of context such that its original functionality is misapplied.

Consequently, since each and every feature of the present claims is not taught (and is not inherent) in Sano, as is required by MPEP Chapter 2131 in order to establish anticipation, the rejection of claims 1-5, under 35 U.S.C. §102(b), as anticipated by Hathaway is improper.

In view of the amendment and arguments set forth above, Applicant respectfully requests the Examiner to consider Sano in its entirety as set forth in MPEP 2141.02(VI) when applying Hathaway in the §102(b) rejection. Further, Applicant respectfully requests reconsideration and withdrawal of the §102(b) rejection of claims 1-5.

3. Conclusion

In view of the foregoing remarks, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is requested that claims 1-5 be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the Applicant's representative, the Examiner is invited to contact the undersigned at the numbers shown.

Respectfully submitted,

STUDEBAKER & BRACKETT PC

/Donald R. Studebaker/  
Donald R. Studebaker  
Reg. No. 32,815

STUDEBAKER & BRAC  
Suite 105  
Reston, Virginia 20191  
(703) 390-9051